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ACOUSTICAL SCANNING OF OPTICAL IMAGES

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Stanford, California 94305

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The parallel research efforts of high barrier height Schottky diodes and Sezawa wave storage correlators have been integrated and storage has been demonstrated with 1 ns pulses. Storage times in storage correlators of 400 seconds have been demonstrated by cooling to -75 C. The initial experiments in flaw discrimination indicate the possibility of discriminating between different size voids, and discriminating between filled and unfilled holes. Broadband (42%) active matching circuits have been implemented and a design is investigated for making active matching circuits without the use of any indicators.

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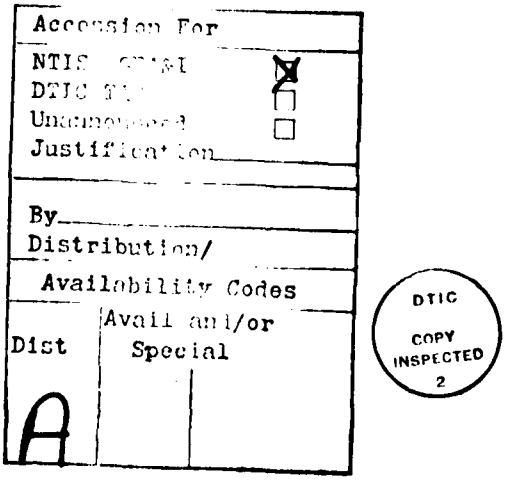


I. MANAGEMENT REPORT

A. Summary

During the last six months, the construction of surface acoustic wave devices has been proceeding slowly since the integrated circuit laboratory has been out of action (due to major repairs on the building), and we have been experiencing problems with the ZnO technology.

The development of active matching networks for SAW devices has now been finished. We have obtained a 42 MHz bandwidth at a center frequency of 100 MHz using a $LiNbO_3$ device. Earlier we obtained approximately 30% bandwidth on ZnO Sezawa mode devices. The matching procedure is relatively simple, and may prove very useful for correlators and convolvers.

Using this technology, on an associated Joint Services contract, we have to develop a so-called SAW/FET ZnO on Si device. This device has the abiiity to read an acoustic surface wave signal into a diode array (as is done in the ZnO/Si storage correlator), and slowly read out the information in the diodes into an external analog or digital memory. Conversely, it is possible to read information into the diodes slowly from an external source and perform the correlation between this signal and a high-frequency signal read into an acoustic port. We envisage that when a storage correlator has adapted to signals read into it, it would then be possible to read out the adapted form of the filter to an external memory, and therefore obtain a permanent record of the adapted function that can be used to refresh the slowly volatile storage correlator. This property will be very useful for our work on pattern recognition, discussed below. An initial SAW/FET has been constructed in the

IC lab and tested in our own laboratory. Preliminary tests have shown that we can read a low-frequency signal into the diode array and read it out as a high-frequency signal on the acoustic ports. Several more devices remain to be tested.

We are currently working on a pattern recognition scheme and are hoping to demonstrate it in NDE applications. The basic idea is to be able to recognize different diameter holes in a metal block, and also to recognize whether these holes are filled with water or not. An acoustic pulse is injected into the block, and the received signal is stored in a surface wave correlator. We train on a known hole and then try to recognize an unknown hole. We would like to have up to one minute of storage time, but to avoid that problem, we are initially using two identical transducers obtained from a medical instrumentation company. The initial results are encouraging.

The ZnO technology has suffered from difficulties in the last six months. As we have described in previous progress reports, we have been able to obtain very high-quality ZnO when deposited on Si and a number of other possible substrates. These results were very repeatable. Recently, however, we had a problem with the magnets in the magnetron head, which led to poor-quality ZnO. We hope to get over this difficulty in the next month.

B. Research Plan

Our aim is to build Sezawa mode, broadband, ZnO on silicon correlator devices using Schottky diodes which can operate with rapid turn-on times, with expected bandwidths of the order of 50 MHz at a center frequency of approximately 160 MHz. These are intended to be used for demonstrations of

removal of interfering signals and distortion, and pattern recognition in NDE applications.

C. Major Accomplishments

New pattern recognition techniques, using the SAW storage correlator, are being investigated. A new storage device with slow read-in/read-out capability is being developed on another contract using the technology developed here.

D. Problems Encountered

Problems with ZnO deposition, as described above.

E. Fiscal Status

Total amount of contract	$899,260
Expenditures & commitments through 12/31/81	$639,310
Estimated funds required to complete work	$259,950
Estimated date of completion of work	14 November 1983

F. Action Required by DARPA/ONR

Better arrangements for receiving and dealing with our reports. Could we not distribute these without having to delay them for reading at DARPA or ONR?

II. ACTIVE MATCHING CIRCUITS

The objective of this work is to develop active matching circuits for surface acoustic wave IDTs. In the previous progress report we presented the design philosophy and reported on some initial results. Since then, a series of improvements in the active filter design have been made and we were able to exceed or equal the best results obtained from passive matching circuits for $LiNbO_3$ IDTs and monolithic ZnO on Si IDTs. Detailed design and performance data are presented in this progress report. A technique for active matching without the use of any inductors is also presented. For the first time completely integrated active matching networks with monolithic Si SAW devices are possible since bulky nonintegratable inductors are eliminated.

The process of driving the IDT from a low-impedance emitter follower source is shown schematically in Fig. 1a, and the complementary receiver process is shown in Fig. 1b. If the source resistance R_s is small compared to the transducer capacitance reactance X_T and acoustic susceptance $B(\omega)$, then the frequency dependence of the power transfer is independent of C_T and $B(\omega)$:

$$P_{ac} = \frac{V^2 G(\omega)}{2} = \frac{V_s^2 G(\omega)}{2} R_s \left(\frac{1}{R_s} + j\omega C_T + jB(\omega) + G(\omega) \right)$$

$$P_{ac} \approx \frac{V_s^2 G(\omega)}{2}$$

Similarly, the power transfer of the receiver is of the same form. Thus, if active compensation circuits are made, which have a frequency-dependent gain $1/G(\omega)$, then the overall response will be flat. This process is represented in Fig. 2.

The acoustic conductance has the dependence

$$G(\omega) = G_{a0}\left(\frac{\sin X}{X}\right)^2 \approx G_{a0}\left(1 - \frac{N^2\pi^2}{3}\Delta^2\right) \tag{1}$$

where

$$\Delta = \frac{\omega - \omega_0}{\omega_0}$$

$$X = N\pi \frac{\omega - \omega_0}{\omega_0} = N\pi\Delta$$

This dependence can be compensated to second order by an amplifier whose gain depends on the admittance of a parallel R-L-C circuit

$$Y(\omega) = \frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right) \tag{2}$$

$$= \frac{1}{R}\left[1 + 2(\omega_0 RC)^2\Delta^2\right]$$

For compensation [compare (1) and (2)] we must have

$$\omega_0 RC = \frac{N\pi}{\sqrt{6}}$$

$$L = \frac{1}{\omega_0^2 C}$$

A voltage amplifier whose transfer function has this characteristic is shown in Fig. 3. The complete circuit including biasing resistors and power connections shown. The rf portion of the circuit is indicated by heavy lines.

This design was tested on a $LiNbO_3$ three finger pair delay line operating at 100 MHz . The results are shown in Fig. 4. The uncompensated response is shown in the upper photo [$G(\omega)^2$ dependence]; the compensation network response is shown in the center photo, and the overall response is shown in the lower photo. A 3 dB bandwidth of 42 MHz was achieved. The same techniques were used with ZnO on Si Sezawa wave delay lines operating at 150 MHz . A 3 dB bandwidth of 42 MHz was again achieved. Complete details of these results are included in Appendix A.

The limitation in bandwidth to 42% was the extent to which the R-L-C circuit matched the frequency response of the IDT. One way to enlarge the frequency response is to use a <u>separate IDT</u> as the load element. In this case, we expect to obtain even better results. The only new requirement is that the transducer impedances for the load be scaled down from the level typical of 1 mm $LiNbO_3$ and ZnO-Si Sezawa wave devices ($R_a \approx 200\ \Omega$) to $R_a < 50\ \Omega$ because of active circuit design considerations. This scaling is easily accomplished by fabricating wider transducers for the load IDTs.

The active matching circuits that would be used in this case are shown in Figs. 5 and 6. These circuits have been constructed. We are presently completing the fabrication of wide IDTs for use with these circuits, and plan to demonstrate these ideas during the next reporting period.

III. MONOLITHIC SCHOTTKY DIODE STORAGE CORRELATORS

A. Schottky Diode Correlators

In our last report, we described various improvements to be made in the design of the Schottky diode storage correlator. These included longer storage times due to higher barrier height diodes (using a technique developed under this contract) and lower spurious signals due to changing the placement of the readout port. Also of concern to us is the successful integration of Schottky diodes into Sezawa mode delay lines that have greater bandwidth due to higher electromechanical coupling. This is necessary in order to utilize more of the inherent bandwidth in Schottky diode devices.

We have therefore fabricated and characterized a Sezawa mode Schottky diode correlator on <111> silicon. The device operates at a center frequency of 149 MHz with a 32 μm wavelength, and has a ZnO layer which is 12.2 μm thick. We have performed correlation experiments with this device and confirmed what would be expected, that it is still possible to store efficiently with a short pulse. The voltages required for storage, however, are significantly larger due to the much thicker ZnO layer. Figure 7 demonstrates this difference in a direct comparison of charge vs. voltage in both a typical Rayleigh mode device and this Sezawa mode device. It should be noted, however, that the voltage levels are still suitable for driving from small, compact avalanche transistor circuits. Complete details on this work are included in Appendix B.

Although this Sezawa mode device exhibited the fast read-in capability, it had two severe drawbacks. Firstly, its relatively poor correlation

efficiency of -97 dBm made it difficult to perform correlation experiments requiring high signal-to-noise ratios. Secondly, the transducers were not optimum for wideband matching networks, although the 15 MHz bandwidth obtained was good for the simple tuning networks used. For these reasons we are, at present, involved in fabricating fully optimized correlators. As described elsewhere in this report, these efforts are being hampered by unexpected difficulties in our ZnO deposition process.

B. Storage Time Increase in Correlators at Low Temperatures

For many possible applications of the storage correlator, it is desirable to have the storage time extended by several orders of magnitude over the values we are presently achieving. For example, in nondestructive imaging applications, one of which we will describe later in this report, it is desirable to have the ability to scan mechanically over a sample for several seconds, or even minutes, with the same reference waveform stored in the correlator. If the reference signal is located physically away from the sample signals to be scanned, the storage time in the device directly determines how much information can be scanned between refreshes.

In order to discover the ultimate storage capabilities within the device, we have experimented with mounting the device in a special dewar which allows us to reduce the device temperature over a wide range, monitoring the device temperature as we go.

Using liquid nitrogen as a coolant, we have been able to cool an operating storage correlator to a temperature of -75°C (198 K). This has resulted in an increase in the storage time from a room temperature value

of 2.4 msec to roughly 405 sec at -75°C . This corresponds to over 5 orders of magnitude increase in storage time. Figure 8 shows the storage time versus reciprocal temperature. These storage times are more than sufficient for the requirements of the acoustic scanning systems presently in our laboratory.

C. Storage Correlator Flaw Discrimination

We have begun a series of experiments to utilize the monolithic storage correlator as a pattern recognition device for flaw discrimination in nondestructive evaluation. In this mode of operation the scattering from a "reference" flaw is stored in the correlator, and correlated with the scattering from various unknown flaws. The degree of similarity between the flaws will determine the available peak correlation output from the correlator.

As an example of the types of variations which can be detected, Fig. 9 shows the scattering by a 3 MHz resonant transducer impulse from a .060" diameter hole drilled into an Al block. In Fig. 9a, the hole is filled with water, and so part of the wave is matched into the water, giving secondary reflections due to signals that propagate in the water and reflect off the back side of the hole. In Fig. 9b the same scattering source, only with the hole air-filled, is shown. Note the dramatic reduction in amplitude of the secondary echoes, now due to "creeping wave" echoes which return after navigating the circumference of the flaw.

With the correlator, we are aiming to make it possible to enhance the sensitivity of the main signal amplitude to the presence or absence of the

secondary signals, thereby allowing threshold type discrimination between different types of flaws or materials filling the flaw.

IV. ZnO TECHNOLOGY

Over the last six months we have had several problems in obtaining well-oriented ZnO films. We used to deposit ZnO films consistently with an excellent orientation: C-axis normal with a standard direction of the x-ray rocking curve of less than $1°$. More recently the standard deviation has been consistently around $2°$, and worse still two to three months ago.

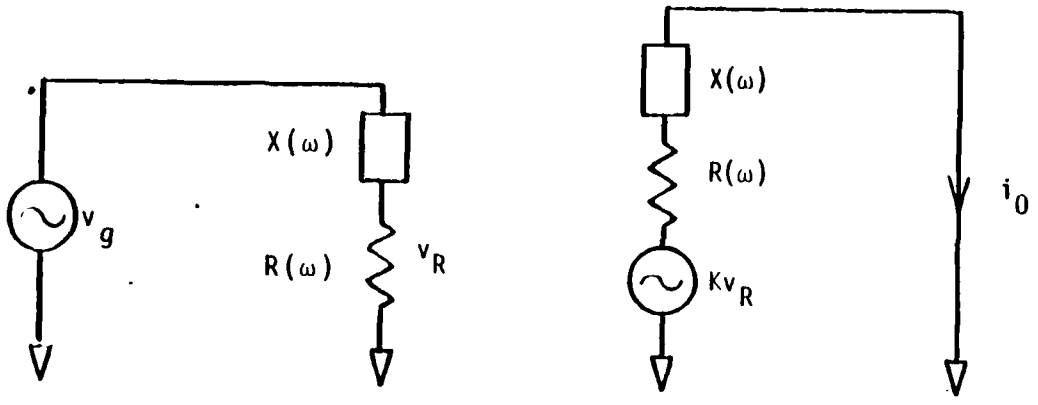
Consequently, during the last six months we have evaluated the performance of every part of the vacuum station. We found a couple of small leaks, cleaned the station, and checked the thermocouple and vacuum gauges. All of the above checks did not provide a cause for the problem we encountered. We attached a residual gas analyzer on the station to see if any impurities were present in the station; again the results were negative. Recently, we decided to change the zinc target. By going through our records, we see a correlation between the start of the manifestation of the problem and the time when the zinc target was recast. It is important to note here that we periodically remelt the zinc into the target as the erosion ring grows deeper into the target. This, of course, is one of the advantages of our system in terms of waste of target material. Our assumption at the moment is that during the last remelt, some impurities got into the target.

We have carried out electron dispersive x-ray (EDAX) analysis of our ZnO films and found no impurities in them. However, the accuracy of EDAX is of the order of 1-2% , and we can indeed have impurities that are not resolvable by this method of analysis. The new target was made, and while in the process of installing it, we found a major problem. The center disk magnet was

broken, and the ring magnet was much weaker. About five months ago we did check to see if the magnets were weakened by measuring the magnetic field over the target. However, we did not get a conclusive answer because of the difficulty encountered in measuring the magnetic field in the vacuum station.

We have ordered new magnets for the magnetron, and we hope to receive them in a couple of weeks. We have also installed the new target because we still are not certain whether the old target had any impurities in it or not. We hope that within a month we will have the system operating under optimum conditions.

LIST OF FIGURES



(a) (b)

Fig. 1.

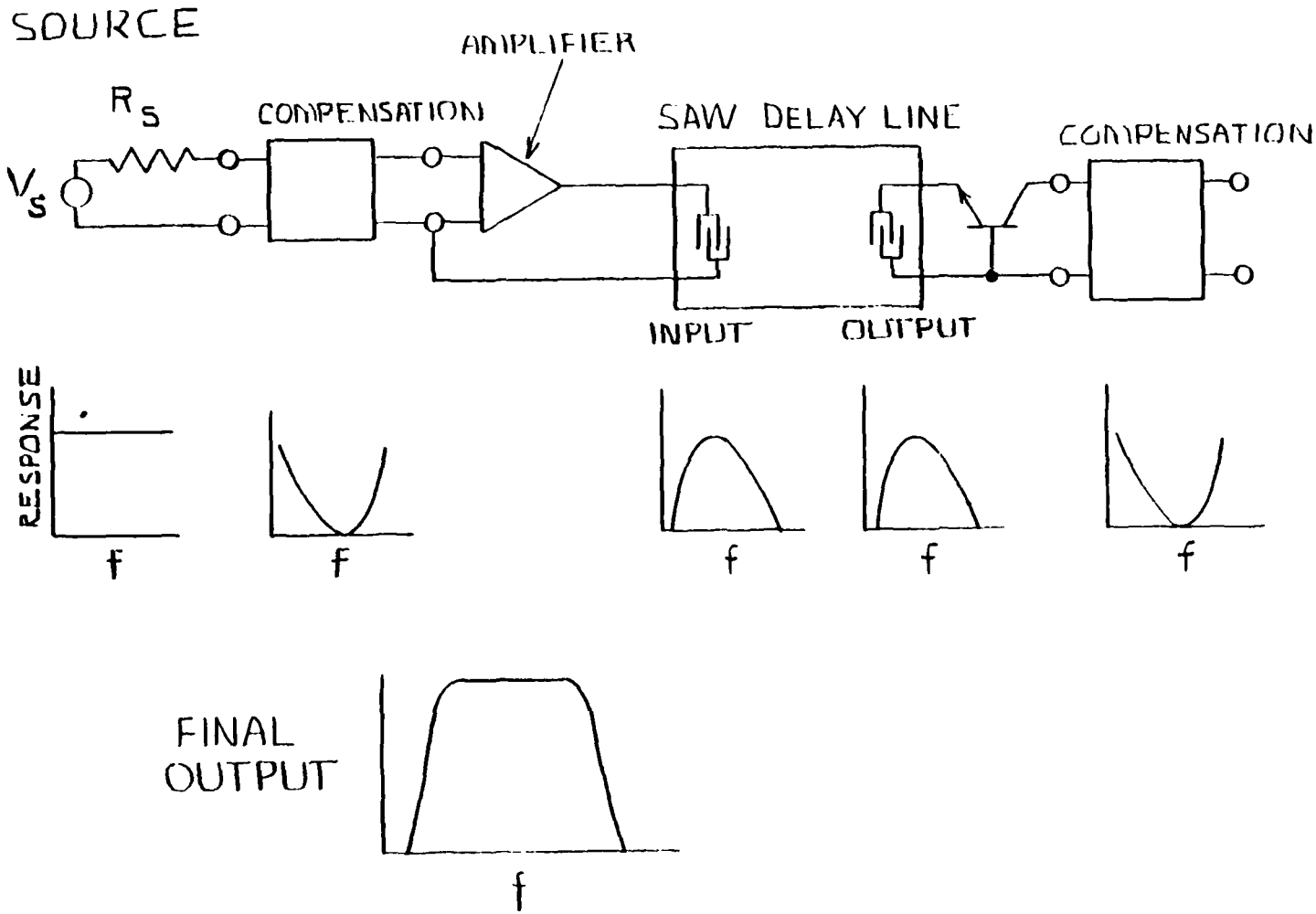

SOURCE
AMPLIFIER
R_S
COMPENSATION
SAW DELAY LINE
COMPENSATION
V_S
INPUT
OUTPUT
RESPONSE
f
f
f
f
f
FINAL
OUTPUT
f

Fig. 2.

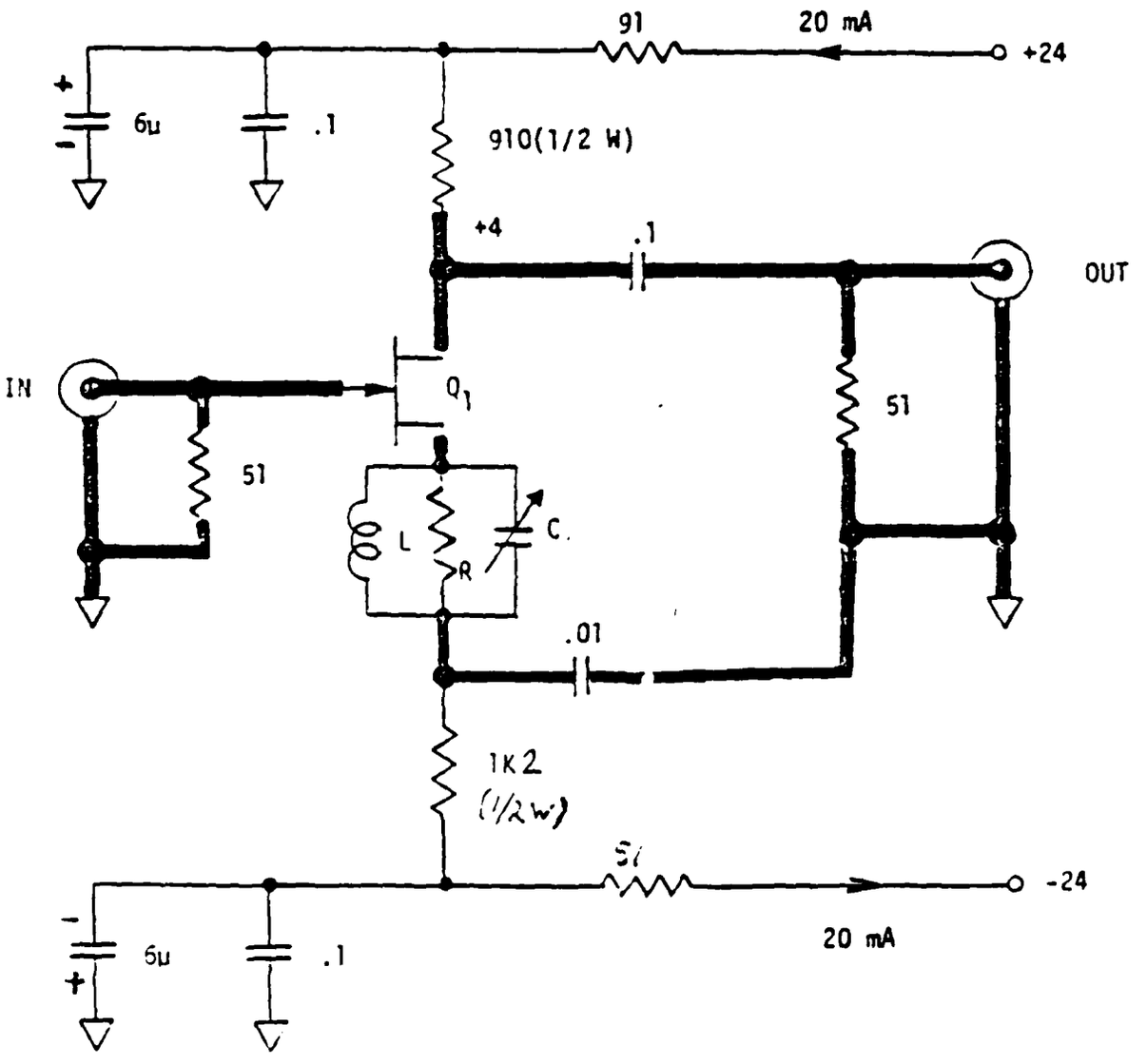
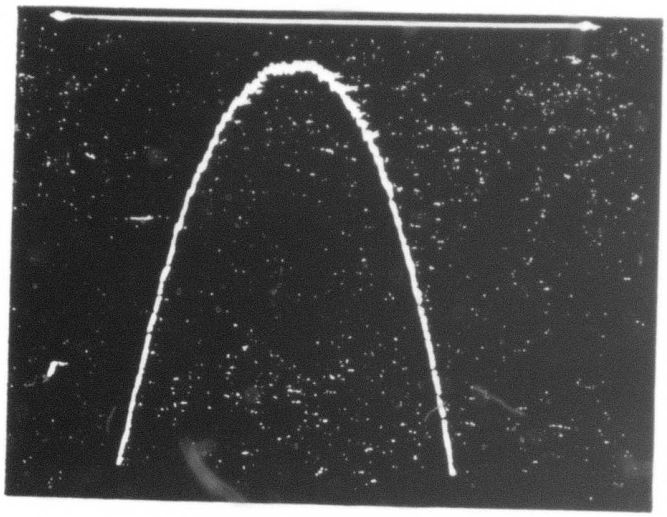
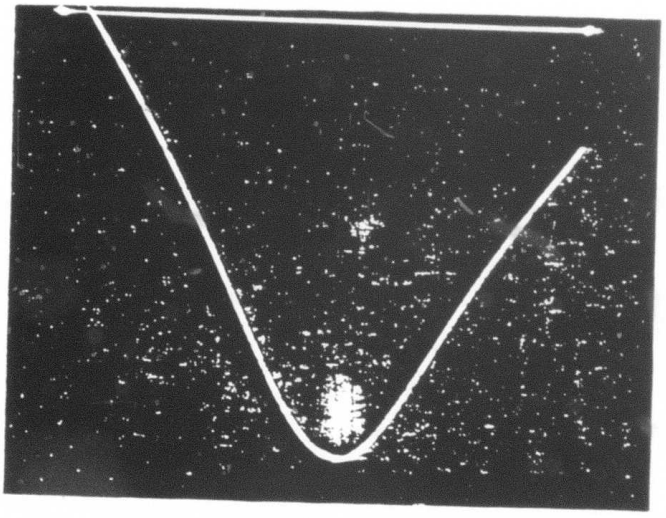

91
20 mA
+24
6u
.1
910(1/2 W)
+4
.1
OUT
IN
Q_1
51
51
L
R
C
.01
1K2
(1/2w)
51
-24
20 mA
6u
.1

Fig. 3.



(a)



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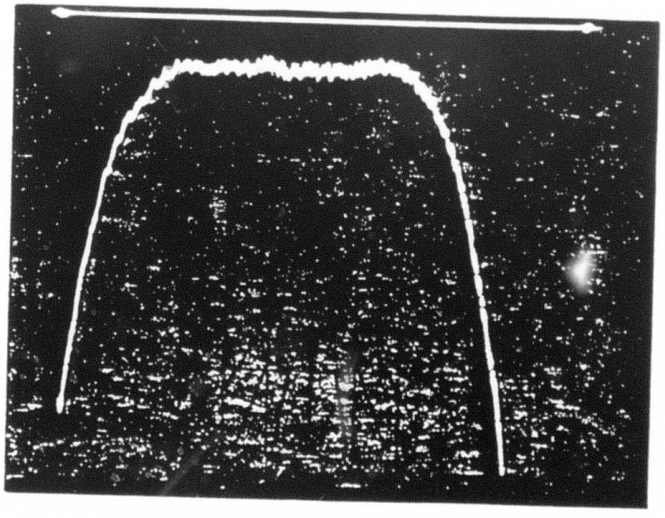


(c)

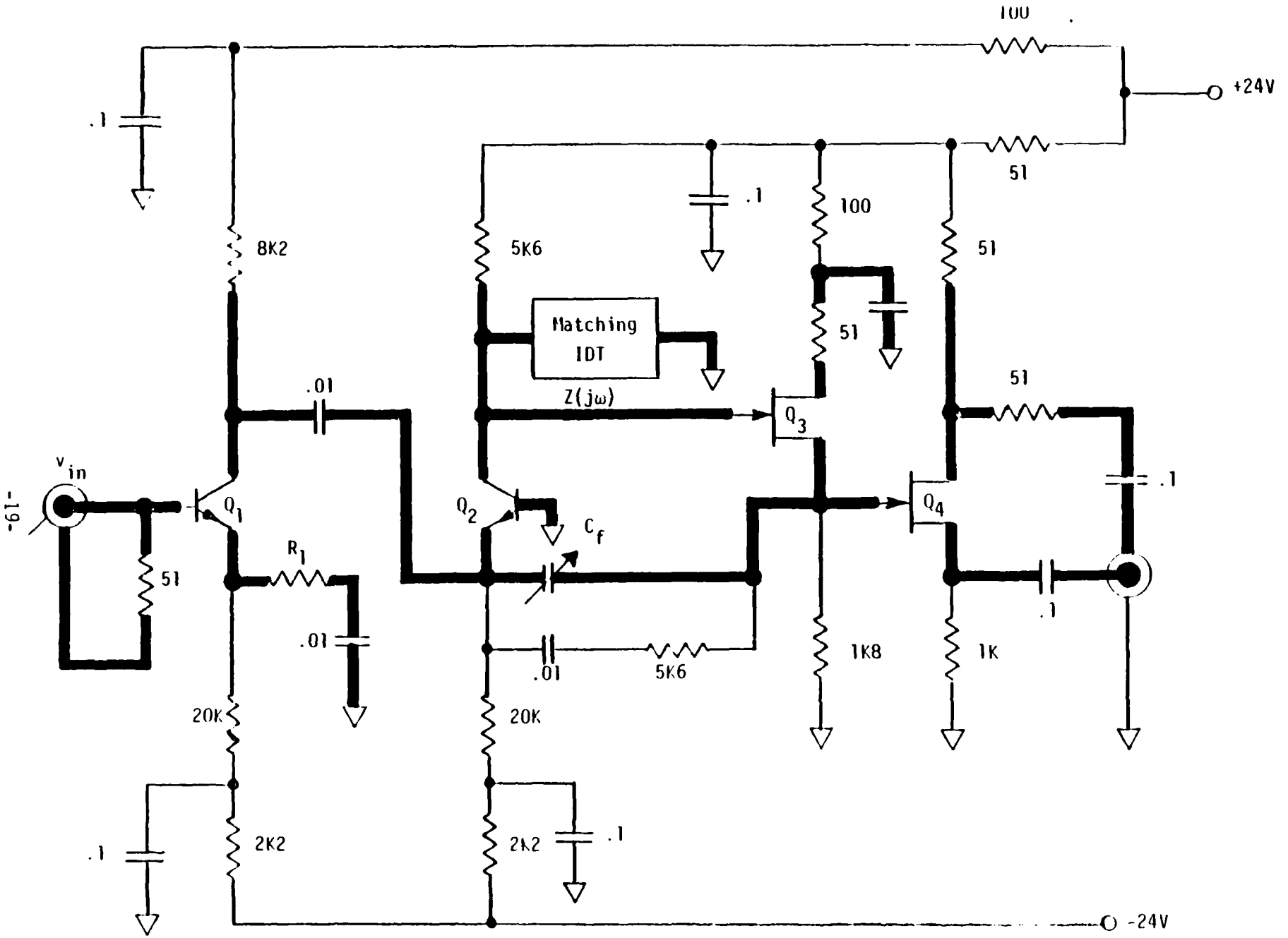
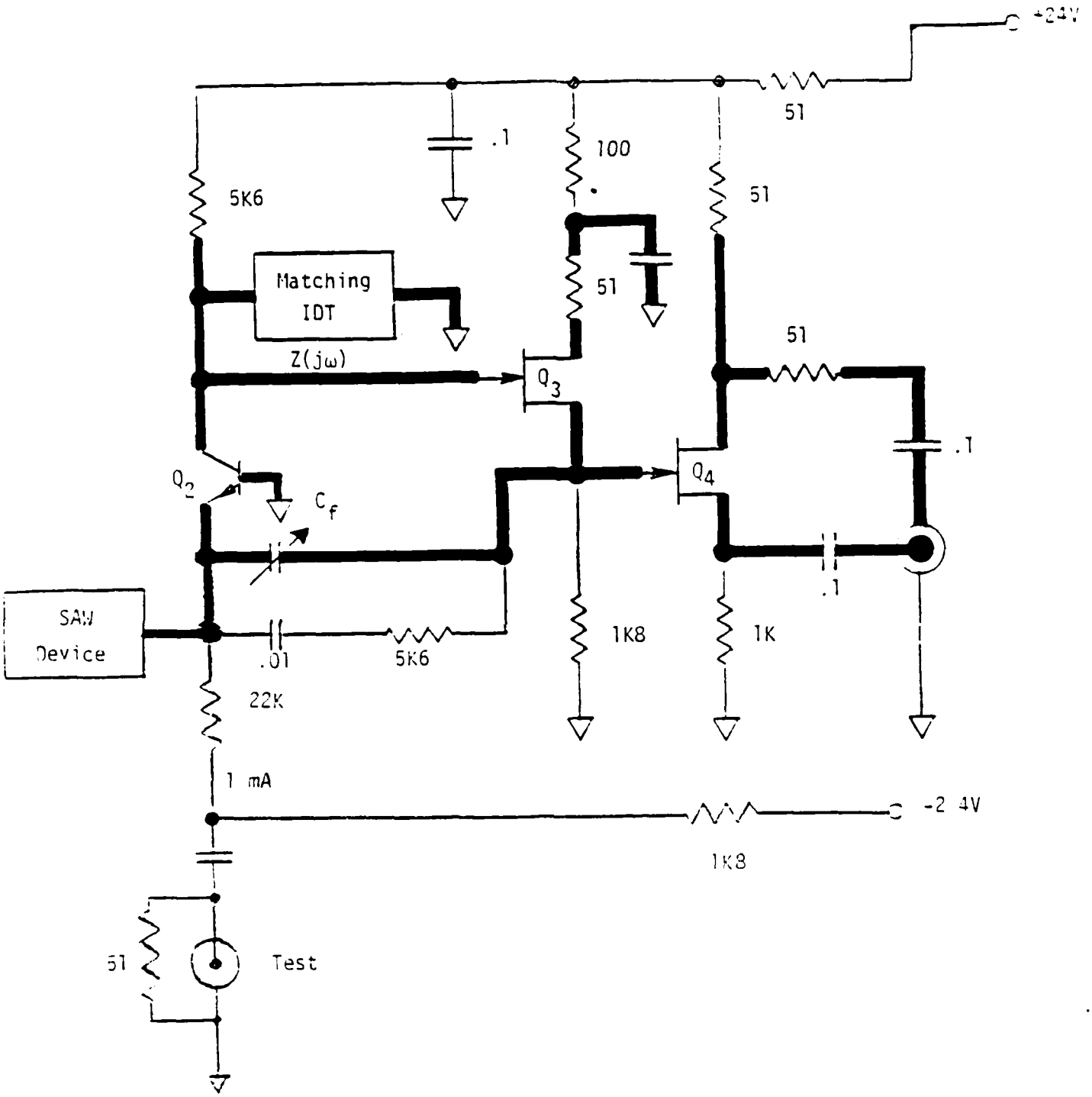

100
+24V
.1
51
.1
100
5K6
51
8K2
Matching
IDT
51
.01
Z(jω)
Q3
51
.1
Vin
Q1
Q2
Cf
Q4
R1
51
.01
.01
5K6
1K8
1K
.1
20K
20K
.1
2K2
2K2
.1
-24V

FIGURE 5.


+24V
51
.1
100
5K6
51
Matching
IDT
51
Z(jω)
Q3
51
.1
Q2
Cf
Q4
SAW
Device
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5K6
1K8
1K
.1
22K
1 mA
-2 4V
1K8
51
Test

Figure 6.

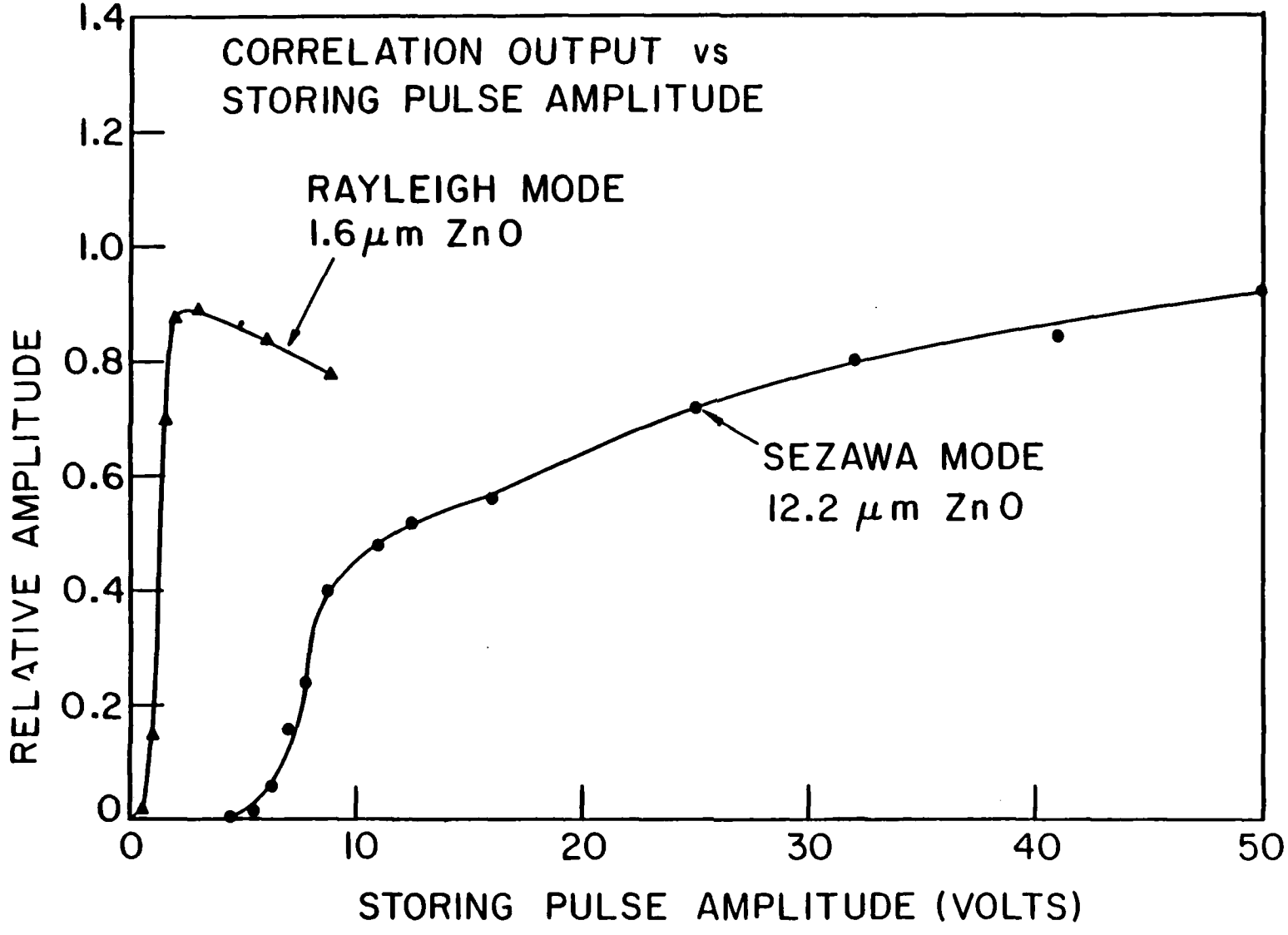

CORRELATION OUTPUT vs
STORING PULSE AMPLITUDE
RAYLEIGH MODE
1.6μm ZnO
SEZAWA MODE
12.2 μm ZnO
RELATIVE AMPLITUDE
STORING PULSE AMPLITUDE (VOLTS)
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
0
10
20
30
40
50

Fig. 7.

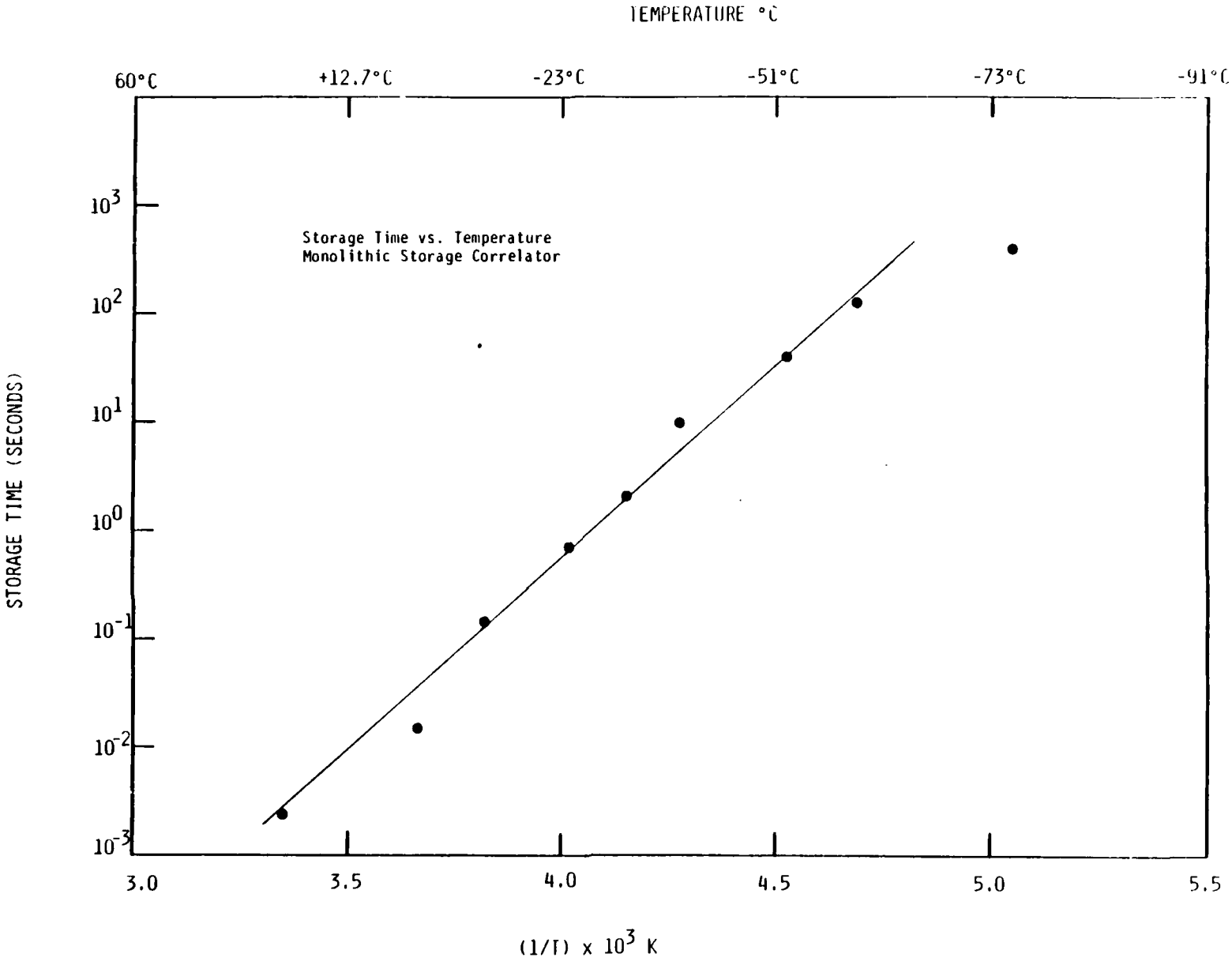
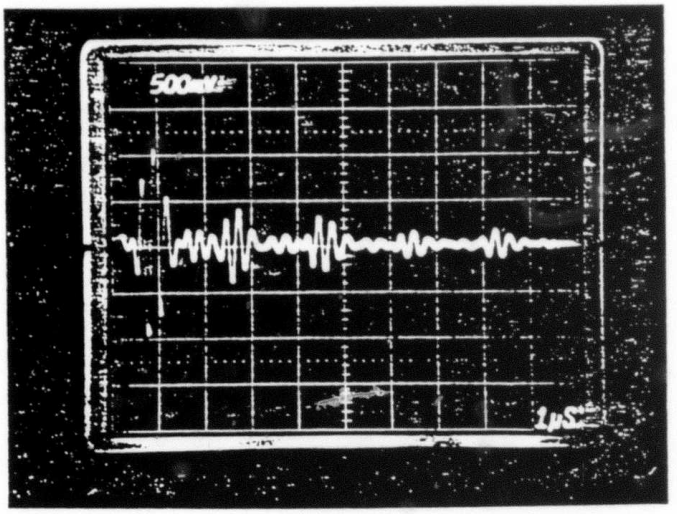
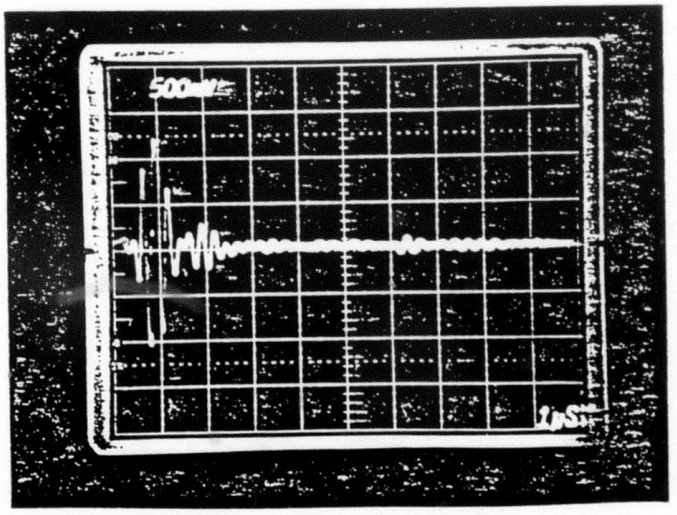

TEMPERATURE °C
60°C
+12.7°C
-23°C
-51°C
-73°C
-91°C
Storage Time vs. Temperature
Monolithic Storage Correlator
STORAGE TIME (SECONDS)
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
3.0
3.5
4.0
4.5
5.0
5.5
(1/T) x 10^3 K

Fig. 8.



(a) with water in hole.



(b) without water in hole.

Fig. 9. Scattering from 60 mil diameter hole.

APPENDIX A

ACTIVE MATCHING OF INTERDIGITAL TRANSDUCERS

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Abstract

Active matching circuits have been developed for matching SAW IDTs to 50 Ω generators and receivers. For the output circuit, the use of a low input impedance receiver allows the elimination of the inductor usually needed to tune out the IDT capacity. The frequency dependence of the radiation admittance is compensated by a single stage active circuit. Similarly, a low output impedance driver with frequency dependent gain is used to directly drive the IDT. A 3 dB bandwidth of 42% has been achieved with $LiNbO_3$ delay lines operating at a center frequency of 100 MHz. The linear dynamic range is 45 dB for $LiNbO_3$ delay lines with active driver and receivers. The dynamic range is 60 dB when a passive input matching circuit is used with a $LiNbO_3$ delay line and an active receiver. Active matching circuits were used with ZnO on silicon Sezawa wave IDTs to achieve 42 MHz bandwidths at 155 MHz. These matching techniques are applicable to IDTs on other materials and also to bulk acoustic wave transducers.

Introduction

Active matching circuits can be employed in principle to compensate for any kind of deficiency in the response characteristic of a signal processing device. The criteria in comparing various methods are the degree of sophistication required to yield a particular result and the signal-to-noise ratio. In this paper, the design considerations for a novel active matching technique will be given and results will be presented for matching to $LiNbO_3$ and Sezawa wave ZnO on Si devices. The approach presented here has the advantages of greater triple transit loss, insensitivity to pad and stray capacities, and broad bandwidth. The need for large inductors that occurs with passive matching to IDTs with small finger capacities is eliminated by the circuits presented here.

Principle of Operation

The electrical admittance of the interdigital transducers considered here can be modeled as a parallel combination of a capacitor (C_T), conductance $[G(\omega) = G_{a0}(\sin x/x)^2]$, and susceptance $[B(\omega) = G_{a0}(\sin 2x - 2x)/2x^2]$, as shown in Fig. 1a. In this model, the shunting effect of the finger capacity dominates the overall response, unless its effect is tuned out at the center frequency by an inductor. The input and output circuit are therefore designed so as to eliminate the effect of C_T and $B(\omega)$ on the transfer function. This is achieved by driving the input transducer from a low impedance source and connecting the output transducer to a low input impedance amplifier. In practice, these impedance levels can be made sufficiently low to consider the input amplifier as a voltage source and the input impedance of the output amplifier as a short circuit. The acoustic power transmitted is

$$P_{ac} = \frac{1}{2} V_s^2 G(\omega) = \frac{1}{2} V_s^2 G_{a0} \left(\frac{\sin x}{x}\right)^2 \quad (1)$$

$$= \frac{1}{2} V_s^2 G_{a0} \left(1 - \frac{N^2\tau^2}{3} \Delta^2\right) \quad (2)$$

where $x = N\pi(\omega - \omega_0)/\omega_0$, $\Delta = (\omega - \omega_0)/\omega_0$, and V_s is the voltage of the source. The objective is then to design a shaping circuit which compensates for the dependence of conductance on frequency. The amplifier used here has a gain which depends on the admittance of a parallel R-L-C circuit

$$Y(\omega) = \frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right) \quad (3)$$

$$|Y(\omega)| = \frac{1}{R}\left[1 + 2(\omega_0 RC)^2 \Delta^2\right] \quad (4)$$

where L and C resonate at ω_0 and Δ is defined above. Consequently, the product $\omega_0 CR$ is chosen so that Eqs. (2) and (4) have the inverse frequency dependence

$$\omega_0 RC = \frac{N\pi}{\sqrt{6}} \quad (5)$$

The receiver circuit can be analyzed similarly. A crossed field Mason model was used[1] with a short at the electrical port (Fig. 1b). The

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ratio of the output current I to the acoustic source V_{ac} is found to be proportional to the radiation conductance $G(\omega)$. Consequently, a second shaping circuit with the same response as above was used to compensate over a limited frequency range for the frequency dependence of the receiver.

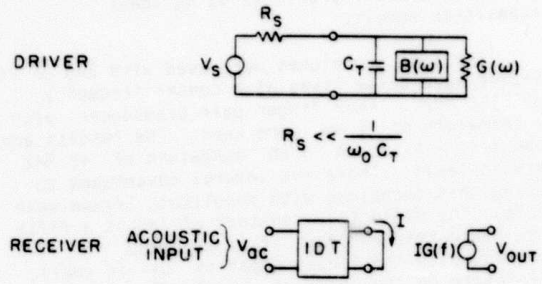


Fig. 1. Schematic diagrams of driver (a) and receiver (b) circuits.

Description of Active Matching Circuits

A class of active filters has been developed, which overcomes the frequency limitations of filters employing frequency selective networks in the feedback path of operational amplifiers, and using two or more transistors within the loop. Instead, a frequency selective element is employed in conjunction with a single transistor operating as a current follower or as a transadmittance amplifier. Feedback is still present in the latter case, but applied around a single transistor only, which extends the frequency response near to the f_T of the transistor.

Two kinds of active filters have been designed. One is a voltage amplifier, and the other one is a transimpedance amplifier exhibiting a low input impedance, suitable to be connected to the output IDT of a SAW device.

Figure 2 shows the voltage amplifier with an RLC circuit as the matching element. The complete circuit, including biasing resistors and power connections is shown. The rf portion of the circuit is indicated by heavy lines. GaAs FET transistors (Mitsubishi MGF 1200) were used. The amplifier transfer function is

$$v_0/v_{in} = R_0 Y(\omega)/2 \qquad (6)$$

The factor of two is due to the output impedance of the FET, which is approximately 50Ω and matches the impedance of the interconnecting cable. The experimental transfer function is plotted in Fig. 3 along with the theoretical prediction (Eq. 3) for R = 940 Ω, C = 7.5 pF and L = .32 μH. The inductor and capacitor were adjusted for maximum 1 dB bandwidth when used with the $LiNbO_3$ delay line receiver described below. The product $\omega_0 RC$ that was actually used is slightly larger (4.5) than the value (3.8) suggested by Eq. (5).

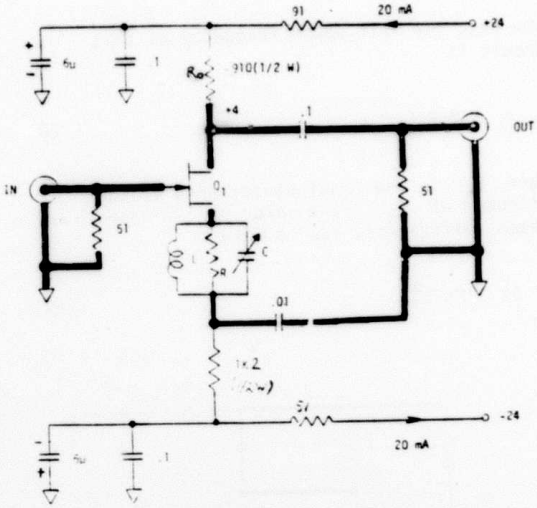


Fig. 2. Voltage amplifier for the driver $G(\omega)$ compensation.

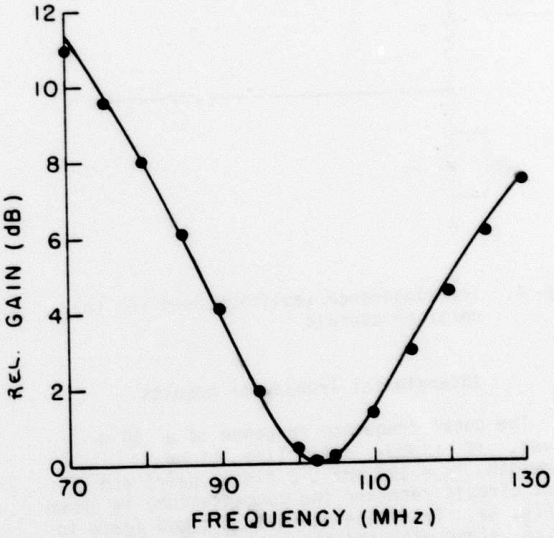


Fig. 3. Transfer function for the network shown in Fig. 2. Experimental data are given by points and the results of Eq. 2 are indicated by a solid line (R = 990 Ω, L = .32 μH, C = 7.5 pF)

The transimpedance amplifier used as the receiver is shown in Fig. 4. Its transfer function is

$$v_0/i_{in} = R_1 R_0 Y(\omega) \quad (7)$$

Note that the half-power frequency of this circuit is

$$f_h = 1/2\pi R_1 C_1 \quad . \quad (8)$$

where C_1 is the total capacitance at the collector of Q_1. The value of R_1 should be chosen sufficiently low to make

$$f_h >> 1/2\pi\sqrt{LC} \quad . \quad (9)$$

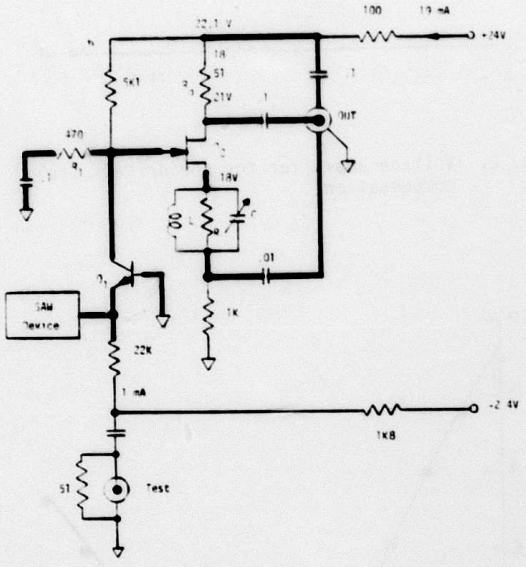


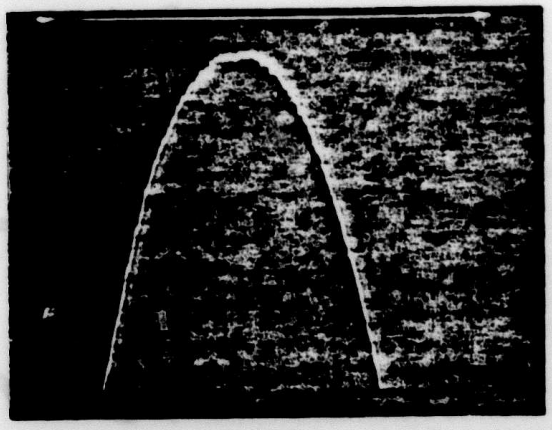
Fig. 4. Transimpedance amplifier used for the receiver circuit

Interdigital Transducer Results

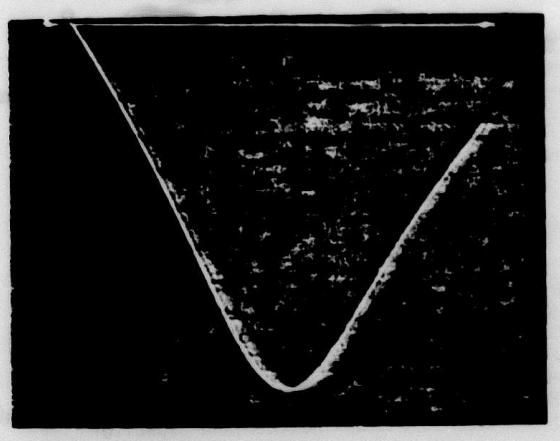
The total frequency response of a 50 Ω driver, YZ $LiNbO_3$ delay line, (1 mm beamwidth, f_0 = 100 MHz, 3 finger pair) and short circuit receiver (no compensation) is shown in Fig. 5a. This dependence is plotted again in Fig. 6, along with the theoretical plot of $G(\omega)^2$ where the theory used N = 2.8. The agreement is very good and thus it can be seen that frequency dependence of $j\omega C_T$ and $B(\omega)$ have been removed by the low impedance driver and receiver.

The response of one of the two compensation stages is shown in Fig. 5b. The overall system response is shown in Fig. 5c. The 1 dB bandwidth is 34 MHz and the 3 dB bandwidth is 42 MHz. This result is plotted in Fig. 7, along with the theoretical prediction (Eqs. 1, 3, 6, and 7). It can be seen that the performance can be accurately predicted using ideal transistor models.

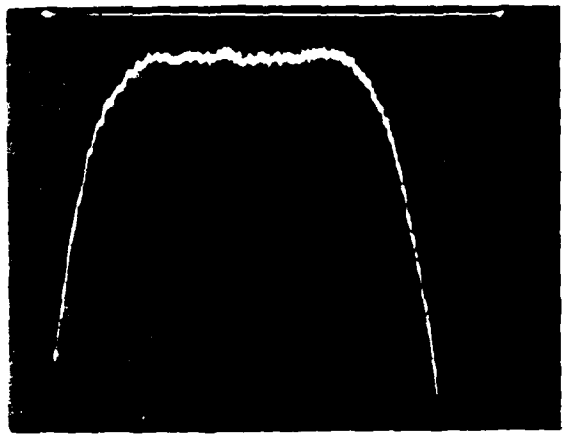
The same techniques were used with ZnO on Si Sezawa wave delay lines at a center frequency of 150 MHz. Four finger pair transducers with a beamwidth of 1 mm were used. The results are shown in Fig. 8. A 3 dB bandwidth of 42 MHz was achieved. There are several advantages to using this technique with monolithic Sezawa wave IDTs. The dielectric constant of ZnO is a fifth the dielectric constant of $LiNbO_3$, and consequently the finger capacity C_T is small; typically on the order of .5 pF for four finger pair, 1 mm beamwidth IDTs. The bonding pad capacity at the IDT and at the inductor is typically larger than C_T, when the device is mounted in a practical package. Consequently, the apparent radiation resistance



(a)



(b)



(c)

Fig. 5. Frequency dependence of $LiNbO_3$ delay line (YZ $LiNbO_3$, w = 1 mm, N = 3, f_0 = 100 MHz) with low impedance driver and receiver. 5 MHz/div, 1 dB/div. (a) response with no compensation; (b) response of one compensating network (Fig. 2) (R = 990 Ω, L = .32 μH, C = 7.5 pF); (c) total response of delay line with the networks shown in Figs. 2 and 3 (R = 990 Ω, L = .32 μH, C = 7.5 pF, R′ = 940 Ω, L′ = 5 μH, C′ = 6.5 pF)

$$R_a = \frac{R_{a0}}{(1 + C_p/C_T)^2} \qquad (10)$$

can be two to four times smaller than the true radiation resistance. The high Sezawa wave coupling coefficient $(\Delta v/v = .028)^2$ is effectively diminished, which results in a reduced bandwidth when passive matching circuits are used. The advantage of the active matching circuits is that the stray and pad capacities do not affect the performance.

A second problem with passive matching circuits is the large value needed for the tuning inductor. ($\gtrsim$ 1.5 μH for the Sezawa wave IDT used here). Inductor self resonance problems are significant for 1 μH and larger inductors at 150 MHz ; the physical size of the inductors is large; and the inductors are sources of undesired electrical pick-up signals. The inductor used in the matching circuit is much smaller and need not be placed in close proximity to the IDT.

Active vs. Passive Methods

A basic disadvantage of this active matching scheme is the signal loss, which is high compared with passive methods in which the capacitor C_T is tuned out at the center frequency. In order to optimize the overall S/N ratio, it is therefore desirable to drive the input IDT at each frequency with the maximum amplitude compatible with linear operation of the SAW device. In cases where the maximum amplitude of the various frequency components falls off at the edges of the useful frequency band, it would be an advantage to employ pre-emphasis shaping in the input channel.

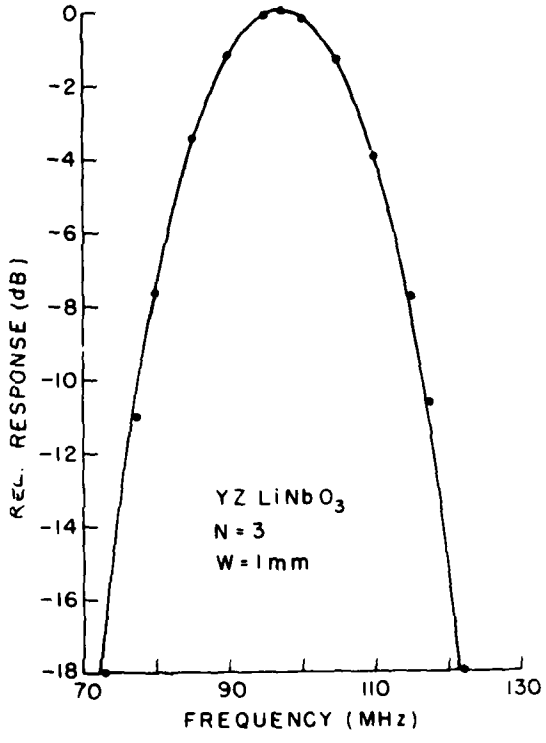


Fig. 6. Transfer function for the $LiNbO_3$ delay line and short circuit driver and receiver. The data of Fig. 5a is represented by points and the result of Eq. (1) is indicated by a solid line.

The dynamic range of the $LiNbO_3$ delay line with a 50 Ω driver and active receiver (Fig. 5c) is 45 dB . The compensation network had an insertion loss of 28 dB at the center frequency and 18 dB at the lower band edge (73 MHz). Additional stages could be added to reduce this loss, or give overall gain to the compensation amplifier.

The use of a 50 Ω source rather than a passive tuning circuit tuned to 50 Ω introduces a loss of 24 dB . This does not reduce the system dynamic range in applications such as memory correlators where the dynamic range is limited by spurious signals rather than thermal noise. Perhaps the best configuration is to use a passive matching circuit for the driver and an active circuit for the receiver. In this case the linear dynamic range was 60 dB .

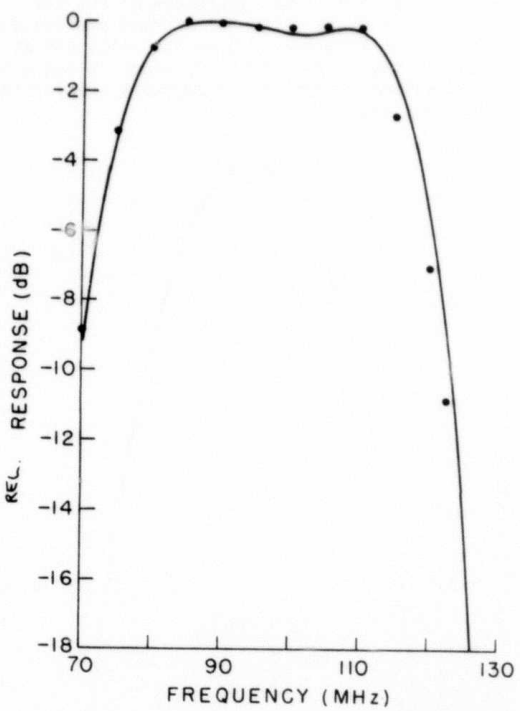


Fig. 7. Total transfer function for $LiNbO_3$ delay line and two compensating networks. The data of Fig. 5c are represented by points and the total theoretical response is indicated by a solid line.

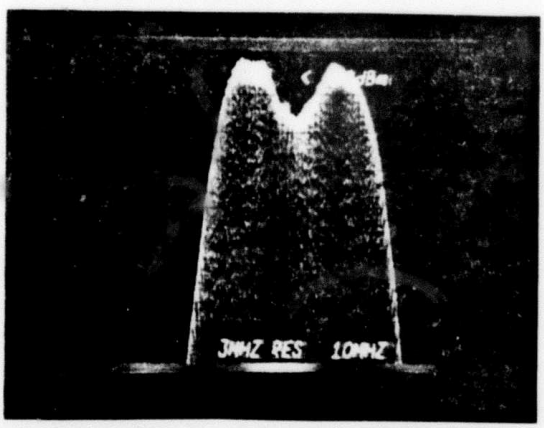


Fig. 8. Experimental result for active matching to a ZnO on Si Sezawa wave delay line (N = 4, w = 1 mm, f_0 = 150 MHz).

A disadvantage of the active approach in some applications is that the matching networks are directional. This is not a problem for convolvers and for many applications of the memory correlator. Note that the active receiver circuit could be used on the plate of the convolver or memory correlator to remove the frequency dependence of the plate capacitor.

The advantages of the active approach in removing the effect of stray capacity and in allowing scaling of the tuning component values have been discussed. A further advantage of active circuits is the reduction of acoustic reflection from the transducer. Gerard[3] has calculated and measured a reduction of 3 dB in acoustic reflection from the IDT when the receiver conductance is increased from the radiation conductance (G_{a0}) to ten times the radiation conductance for resonant loads.

A final advantage of active matching to IDTs on silicon or gallium arsenide substrates is the possibility of integration of the circuit onto the substrate. The circuit configuration used here is not the most advantageous for integration due to the use of FET and bipolar transistors, but other configurations are being investigated. We are also investigating active matching circuits which do not require any tuning inductors and might be fully integrated onto the substrate.

Acknowledgment

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APPENDIX B

RECENT DEVELOPMENTS IN THE ZnO ON Si STORAGE CORRELATOR

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Abstract

We describe improvements in the structure of the monolithic storage correlator. Three areas of improvement open to these devices are bandwidth, storage time, and spurious signal level. We have investigated all of these areas.

We have fabricated Sezawa wave Schottky diode correlators. This allows us, with proper tuning, to obtain 20-30% bandwidths with 1 ns read-in time Schottky diodes. We have succeeded in raising the barrier height of PtSi on Si Schottky diodes from .86 volt up to 1.0 volt by ion implantation. This will dramatically increase device storage times.

We have developed a technique for suppressing the spurious acoustic signals generated by the top-plate during the read-out process. This technique places the top-plate outside of the acoustic beam path and not on the ZnO, thus eliminating any spurious signals generated by the edges of the top plate.

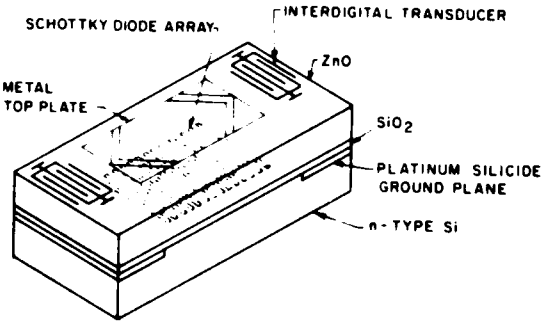

Fig. 1. Monolithic ZnO on silicon storage correlator.

Introduction

The monolithic storage correlator has in recent years become an increasingly attractive device for analog signal processing in the VHF and UHF regions. The fundamental concept of this device has been demonstrated using both pn diodes[1,2] and Schottky diodes.[3] Figure 1 shows the basic structure of the Schottky diode storage correlator. We have demonstrated wide bandwidth correlators using pn diodes for storage elements[4] as well as Schottky diode devices with a 1 ns read-in time capability.[3] In this paper we describe various improvements in these basic structures that extend the signal processing power of the monolithic storage correlator. These improvements address the areas of device bandwidth, device storage time, and spurious signal level suppression.

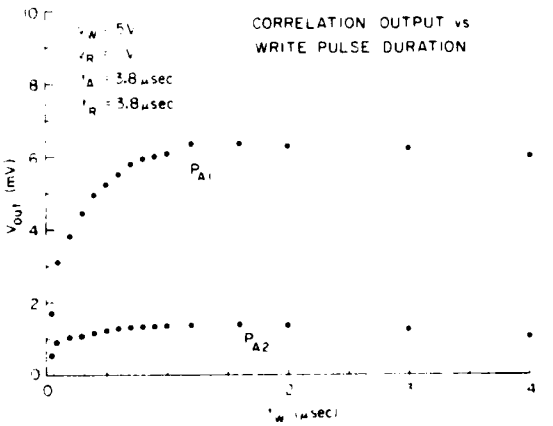

Fig. 2. Relative correlation efficiency of a p-n diode storage correlator as a function of writing pulse duration.

Device Bandwidth

Due to recombination time effects in pn diodes, the effective device bandwidth can be much less than the delay line bandwidth in some important applications. The dependence of storage efficiency on the duration of the rf writing pulse is shown in Fig. 2 for a pn diode Sezawa wave storage correlator. It can be seen that the length of the pulse must be at least 200 ns if the full dynamic range of the correlator is to be used. The bandwidth of the pn diode correlator shown in Fig. 3 is 42 MHz, which is much larger than the effective bandwidth imposed by the 200 ns diode writing time. It is therefore of primary interest to combine the Schottky diode technology with the wideband

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Sezawa mode correlator technology to achieve a device with wideband operation limited only by the bandwidth of the interdigital transducers involved.

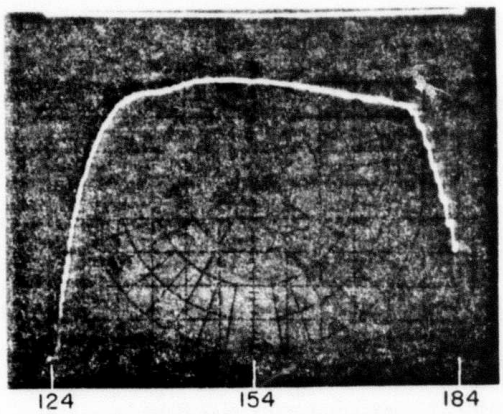

Fig. 3. Delay line bandwidth of Sezawa mode correlator. 5 MHz per horizontal division; 5 dB per vertical division; and 154 MHz center frequency.

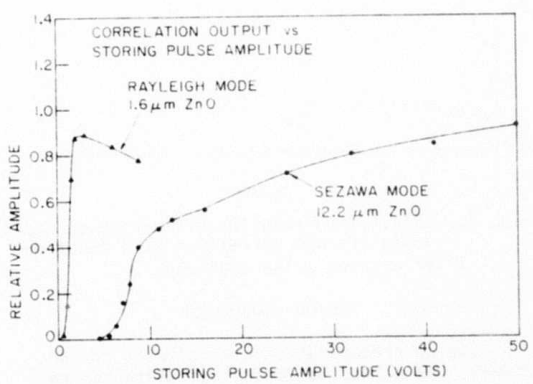

Fig. 4. Relative correlation output as a function of input pulse amplitude for Rayleigh mode (1.6 μm ZnO) and Sezawa mode (12.2 μm ZnO) correlators.

We have designed Sezawa mode ZnO on Si Schottky diode storage correlators on <11> silicon. The film thickness is selected to be 12.2 μm in order to efficiently couple into a Sezawa mode with an acoustic wavelength of 32 μm . This film is almost eight times the thickness of the ZnO in the Rayleigh wave correlator, and we therefore would expect the charging voltage of these devices to be significantly larger, but the impedance level of the plate electrode also to be increased.

We have fabricated ZnO on Si storage correlators using the parameters given above, and we have characterized the dependence of the correlation output signal on the voltage pulse applied to the top-plate to perform the storage operation. The device operates at a center frequency of 154 MHz , and the storing pulse used is ~3 ns wide, or one half of one rf cycle. Figure 4 shows the resultant charging as a function of voltage for the Sezawa wave device, along with a similar curve for a Rayleigh wave storage correlator (ZnO thickness is 1.6 μm). As can be seen from this graph, significantly larger voltages are required to perform the storage operation in the Sezawa mode correlator. This is somewhat of a drawback because of the larger demand put on the pulser used; however, standard avalanche transistor pulse circuits can still be used as drive sources.

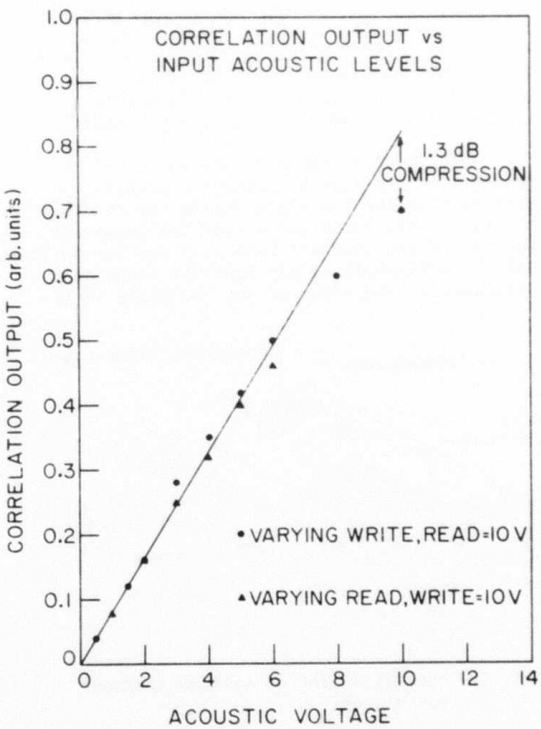

Fig. 5. Relative correlation output for varying read and write voltage amplitudes, showing saturation at high acoustic levels.

In order to investigate the linearity of the correlator output, we have plotted the correlation output at constant storing pulse amplitude, first holding the acoustic read signal constant and varying the acoustic write signal,

and then holding the acoustic write signal constant and varying the acoustic read signal. The results of these two experiments are shown in Fig. 5. We can see that for small acoustic signals, the relations are both quite linear, whereas for voltages larger than about 6v , some nonlinear effects become evident. This efficiency compression has several possible sources. First, the acoustic amplitudes being stored are large, comparable, in fact, to the level of reverse bias on the diodes. It would therefore be expected that small signal linearized theories would begin to break down.

Another possible source of the efficiency compression is insertion loss saturation. Due to the larger thickness of the ZnO layer, it is possible to apply quite large rf voltages to these transducers without dielectric damage. We have looked for an increase in insertion loss with power level by applying +35 dBm pulses to these transducers. There is some evidence of increased insertion loss at these high power levels, accounting for 1 dB of compression in the correlation output at 10 v . This agrees quite well with the amount of compression actually seen, and we therefore conclude that a significant part of the nonlinearity evident in the correlation output curves is indeed due to saturation effects, although we cannot completely eliminate higher order nonlinearity in the charge storage diodes. We should also note here that the ability to apply larger amplitude signals to the acoustic ports also extends the dynamic range of the device.

Device Storage Time

We have performed experiments to demonstrate a technique for raising the effective barrier height for platinum-silicide on silicon Schottky barrier diodes. The technique involves modification of the space charge layer in the PtSi/Si interface.[5,6] The basic concept is described in Fig. 6. In this figure we show the shape of the conduction band in the vicinity of the interface for three different cases.

In case 1, with uniform doping, we have the normal Schottky barrier height. In case 2, where we have implanted a thin n-type layer. the surface electric field is higher, resulting in a barrier of the same height but thinner, allowing the tunnelling component of the current to increase. This results in a lowering of the effective barrier height.

Finally, in case 3, which is the situation of most interest in our devices, we have a narrow p-type region at the interface. This p-type region reverses the sign of the interface electric field, thus causing the conduction band potential to increase away from the interface rather than decrease. The potential that electrons must cross in order to conduct is thereby increased, increasing the effective barrier height for the diodes.

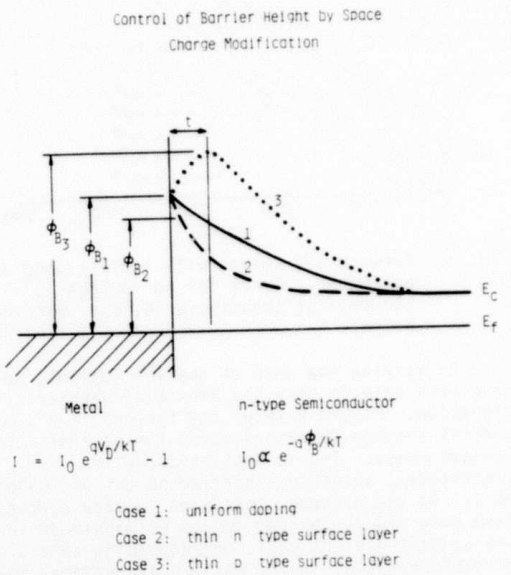

Fig. 6. Modification of the shape of the conduction band edge in the vicinity of the metal-semiconductor interface by narrow space-charge regions.

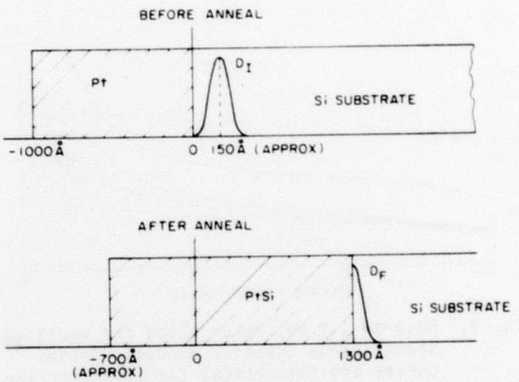

Fig. 7. Boron implant distribution before and after silicide formation, demonstrating pile-up effect resulting in a narrow p-type layer at the interface.

In order to achieve the narrow interfacial p-type layer required, we have used the technique described in Fig. 7, where a shallow ion-implant is performed, followed by platinum metal deposition and silicide formation.[7] As can be seen in the figure, part of the boron is "snowplowed" ahead of the implant, forming the desired narrow interfacial p-type region needed for barrier elevation.

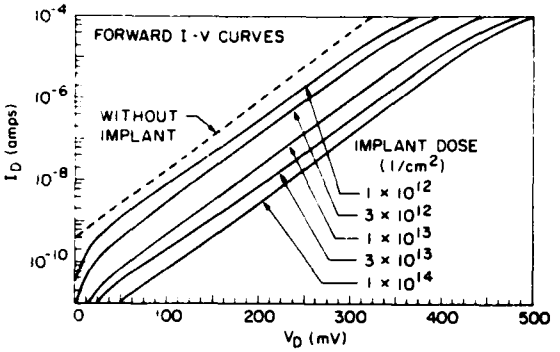

Fig. 8. Forward I-V curves with implant dose as parameter. Curve for no implant is theoretical assuming a 0.86 v barrier height.

By varying the dose of the ion implant, we have been able to vary the amount of barrier elevation. Figure 8 shows the forward current-voltage characteristics for several implant doses. The no implant curve is theoretical, assuming a barrier height of 0.86 volt. As can be seen, the diode leakage currents have been reduced by two orders of magnitude in the highest implant case, corresponding to a barrier height of 1.02 volt. Furthermore, the linearity of these characteristics indicates that the diodes are close to ideal, with n factors ranging from 1.02 to 1.04 .

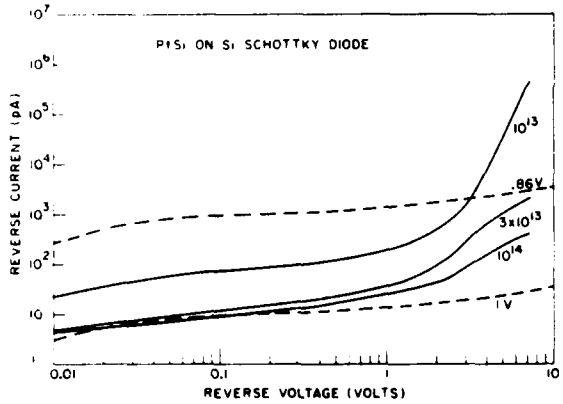

Fig. 9. Reverse I-V characteristics for modified space charge Schottky diodes. Dashed curves are theoretical for given barrier height. Solid curves are experimental for given implant dose.

More important than the forward characteristics, Fig. 9 shows the reverse leakage current in these diodes. Here again we see a dramatic reduction in leakage current. Also shown are theoretical curves for barrier heights of 0.86 v and 1.0 v . We can see that the agreement with theoretical characteristics is quite good at small voltages, corresponding well to the forward characteristics. The increase in leakage at higher voltage levels can be attributed in part to the edge leakage currents.

We thus conclude that this technique is a viable one for barrier height elevation. Projected increases in storage times using this technique are to the point where they are comparable to the storage times in low leakage pn diodes. This is possible while still retaining the fast 1 ns read-in of which Schottky diodes are capable.

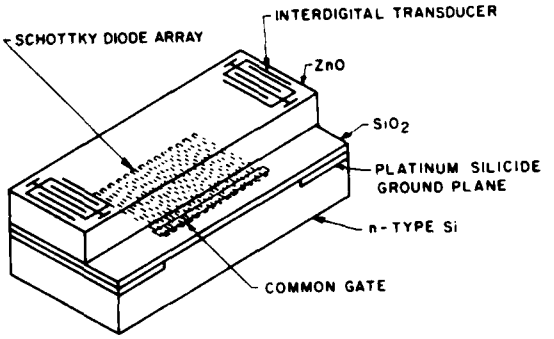

Fig. 10. Modification to storage correlator geometry to reduce spurious signal level.

Improved Correlator Design

Our previous work on monolithic storage correlators has led us to the development of a new design that promises an increase in efficiency and signal-to-noise ratio. A schematic of this new storage correlator is shown in Fig. 10. It is seen that the dominant difference between this device and the previous design depicted in Fig. 1 is that the top-plate electrode has been moved so that it is adjacent to the acoustic beam rather than colinear with the interdigital transducers. Additionally, it is observed that there exists no zinc oxide under the offset top-plate electrode. The top-plate metallization is directly on top of the sputtered SiO_2 layer.

The major advantage of this top-plate structure is the spurious signal suppression afforded by the removal of the top-plate from the acoustic beam path and, as importantly, removing ZnO from the vicinity of the high electric fields on the top-plate.

The spurious signals generated by the reading signal are the dominant factor limiting the input dynamic range. The spurious signals generated when the top-plate is pulsed are shown in Fig. 11 for a normal Sezawa wave device. All of the signals are surface waves. All bulk wave feedthrough was removed by bonding the silicon to a brass box with indium solder. The first signal in Fig. 11 is the rf capacitive pick-up by the IDT. This signal can be further reduced with better shielding. The second signal is due to the excitation by the end of the slanted

top-plate. The large signal which occurs after 2.5 μs is due to a visible defect in the ZnO layer. The series of small signals has a period of 100 ns , which is the same as the period of the step and repeat pattern used for generating the diode fabrication mask.

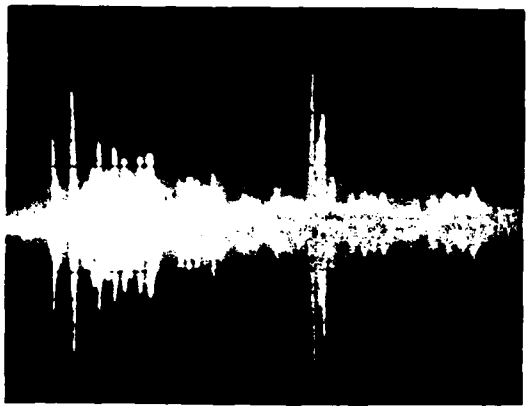

Fig. 11. Spurious signal response at transducer for a short impulse incident on the top-plate .5 μsec per vertical division. Largest signal is 40 dB below correlation output at full amplitude writing voltage.

We are presently fabricating devices using computer generated masks which were not step and repeated. The defect density in the ZnO layer can be reduced by better sample cleaning and cleaning of the ZnO sputtering system. However, moving the top-plate to the region adjacent to the ZnO, as described above, will reduce all of these spurious signals, thereby greatly increasing the dynamic range of these devices.

A further advantage to this structure is related to the fact that we have eliminated the thick dielectric layer between the diodes and top-plate. During the writing process, the top-plate electrode only serves to provide a synchronous bias voltage which adds to the voltage generated by the acoustic wave propagating in the piezoelectric zinc oxide. In the previous correlator design (Fig. 1), the bias voltage was capacitively coupled to the diode array through the capacity provided by the zinc oxide layer. Due to the fact that this zinc oxide is relatively thick (in order to provide good electromechanical coupling), a large voltage drop appears across it. The new correlator design (Fig. 11) circumvents this problem by eliminating the thick zinc oxide layer underneath the top-plate electrode, thus providing a larger capacitive coupling to the Schottky diode array. Therefore, a smaller top-plate voltage is necessary in order to achieve the same voltage at the diodes. This leads to a higher device efficiency.

It is essential that the diode be a metal, such as PtSi, rather than a p-type region in order to minimize RC time constant losses along the length of the diodes. If we consider the diodes as a distributed RC line,[8] we come to the conclusion that a PtSi diode strip 4 μm wide, 1 cm long and ~15 μm thick on silicon of $N_D = 4 \times 10^{14}/cm^3$ would have a time constant on the order of .1 ns , whereas a p-type region with the same length and width, and 1.0 μm thick would have an RC time constant of 10 ns for a relatively high p+ dopant density.

During the read-out process, the new correlator design again is more efficient due to the higher capacitive coupling between the top-plate electrode and the underlying diodes.

Conclusions

In conclusion, we have addressed the three major deficiencies in device performance for the ZnO on silicon storage correlator, device bandwidth, device storage time, and spurious signal level.

We have demonstrated that Schottky diodes can be successfully integrated with Sezawa mode delay lines to achieve the stronger electromechanical coupling and wider bandwidth of Sezawa mode operation.

We have also demonstrated that the barrier height of PtSi on silicon Schottky barriers can be modified to give a higher effective barrier height, thus reducing the diode reverse leakage current and dramatically increasing the storage time possible in the diodes.

Finally, we have suggested a technique for reducing the amplitude of the spurious acoustic signals that are generated during the read-out process. Since these signals are at present the dominant source of spurious output, this technique promises to dramatically increase the dynamic range in the monolithic storage correlator.

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